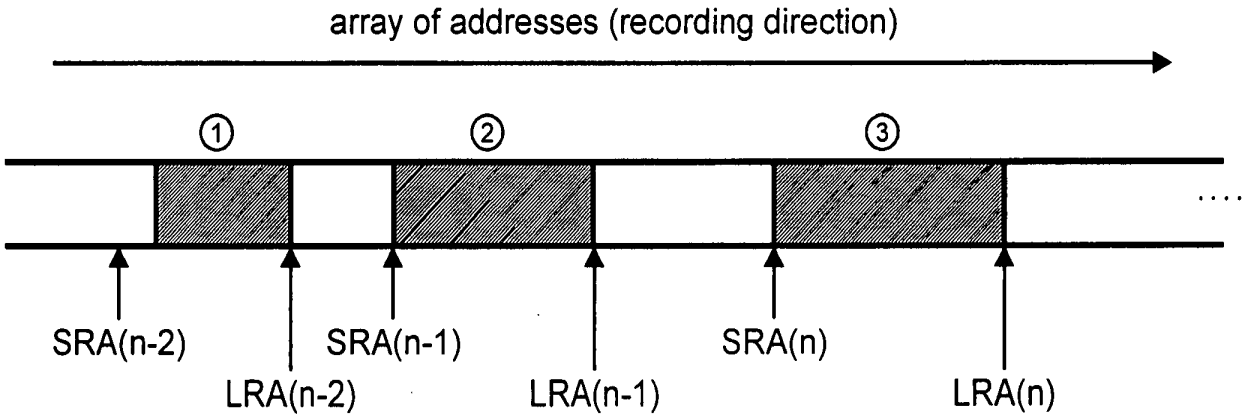
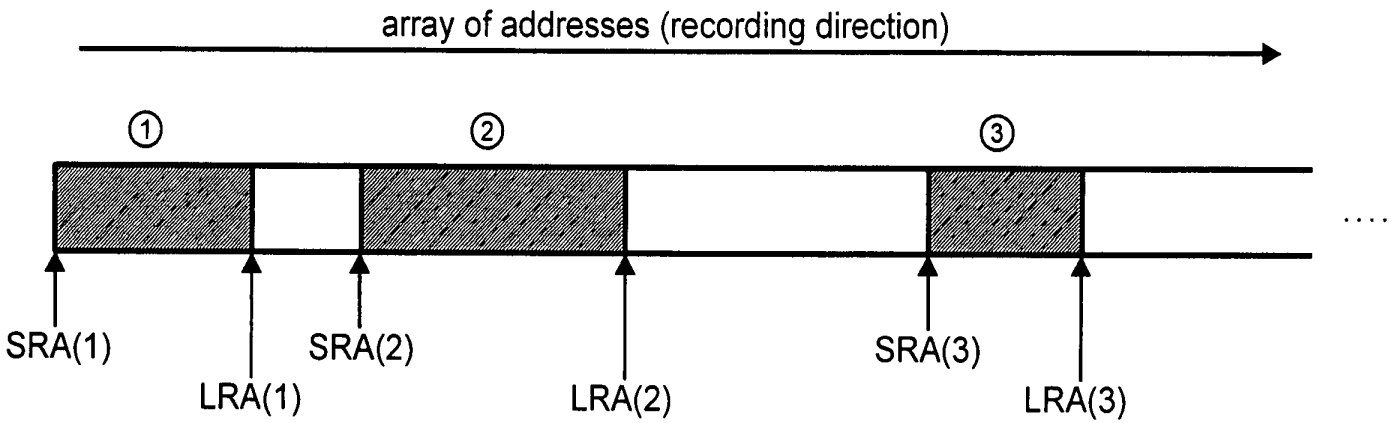
FIG.1



	start address	end address
1	SRA(1)	LRA(1)
2	SRA(2)	LRA(2)
3	SRA(3)	LRA(3)
⋮		
n-2	SRA(n-2)	LRA(n-2)
n-1	SRA(n-1)	LRA(n-1)
n	SRA(n)	LRA(n)

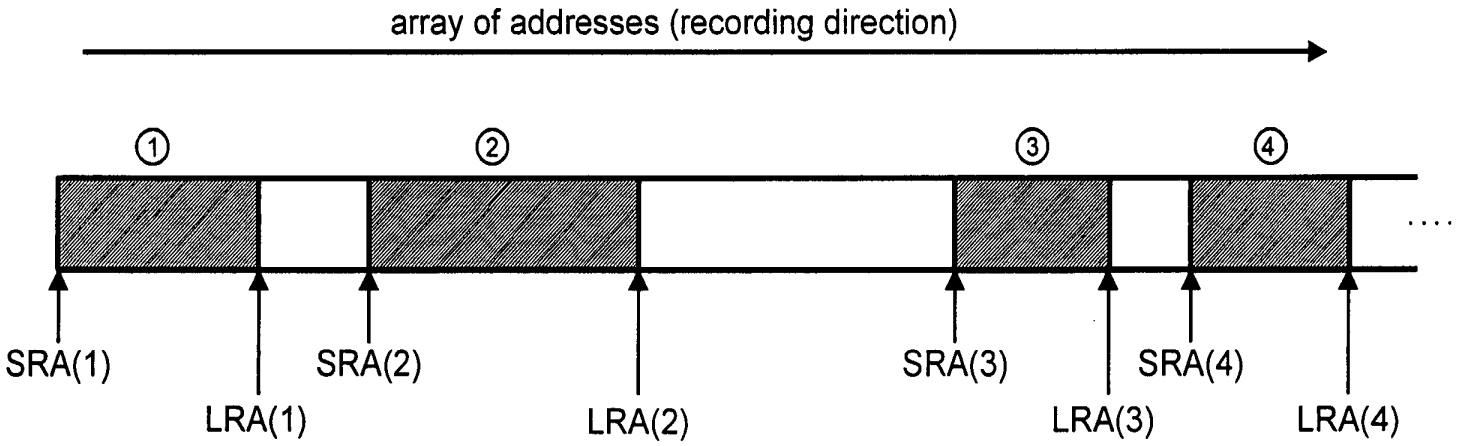
FIG.2



recorded/ unrecorded area management table

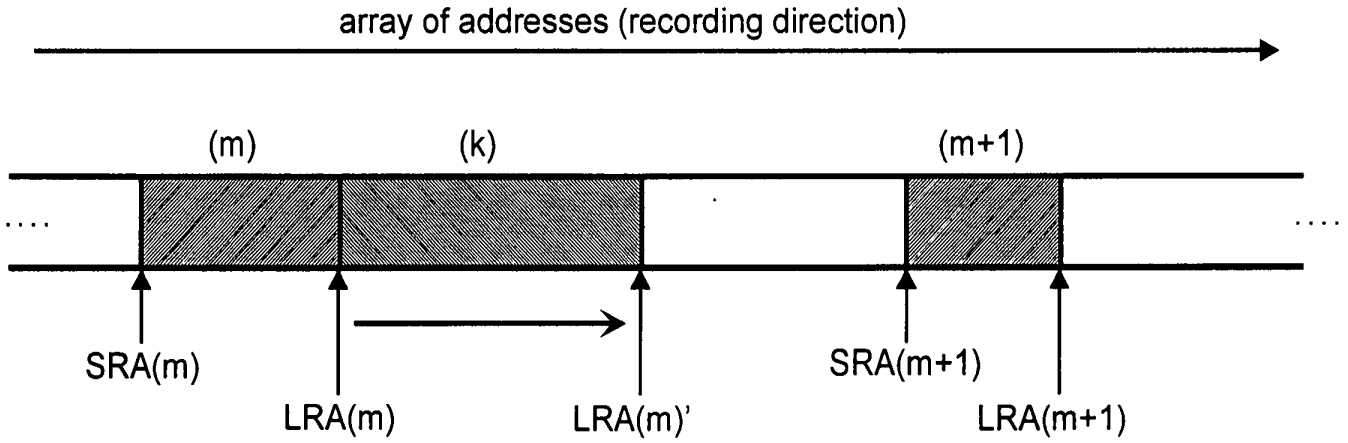
area	start address	end address
1	SRA(1)	LRA(1)
2	SRA(2)	LRA(2)
3	SRA(3)	LRA(3)

FIG.3



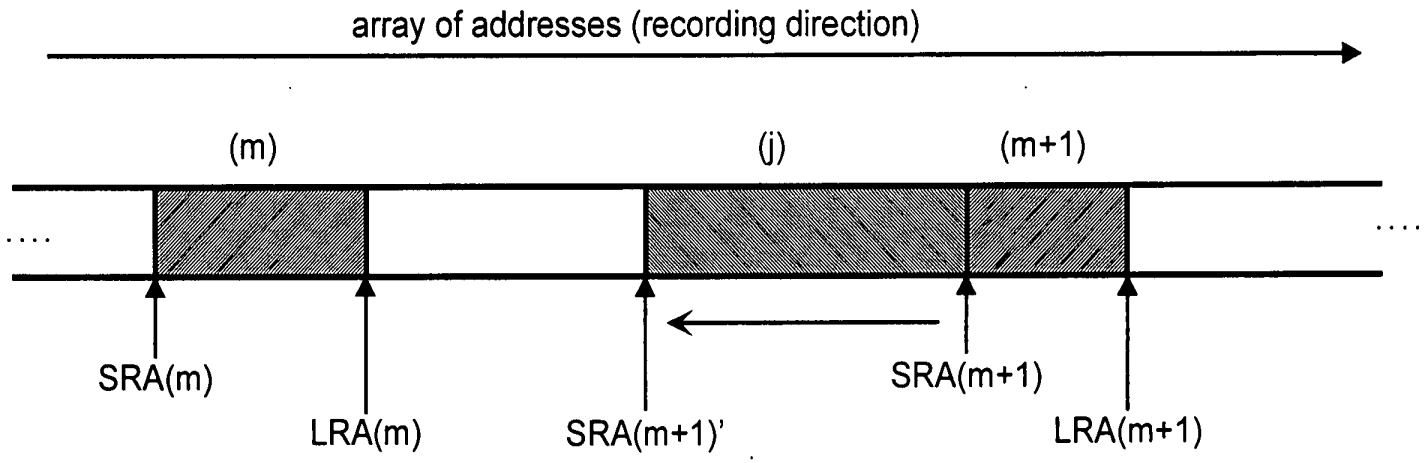
area	start address	end address
1	SRA(1)	LRA(1)
2	SRA(2)	LRA(2)
3	SRA(3)	LRA(3)
4	SRA(4)	LRA(4)

FIG.4



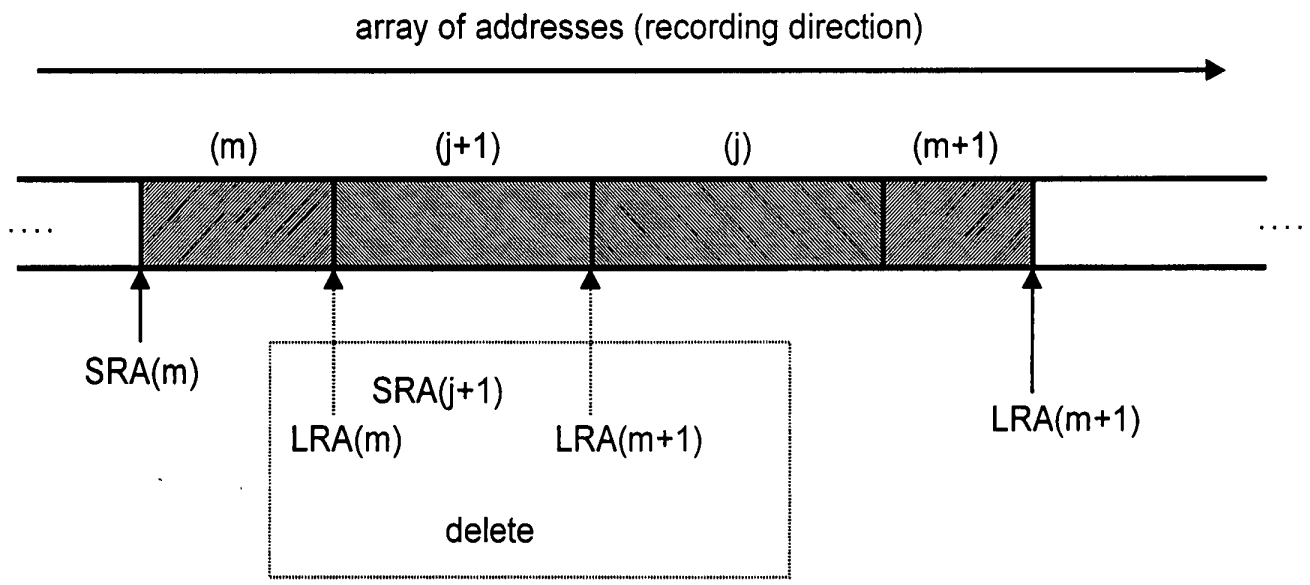
area	start address	end address
m+k	SRA(m)	LRA(m)'
(m+1)	SRA(m+1)	LRA(m+1)

FIG.5



area	start address	end address
m	SRA(m)	LRA(m)
(m+1)+j	SRA(m+1)'	LRA(m+1)

FIG.6



area	start address	end address
m+(j+1)+ j+(m+1)	SRA(m)	LRA(m+1)

FIG.7

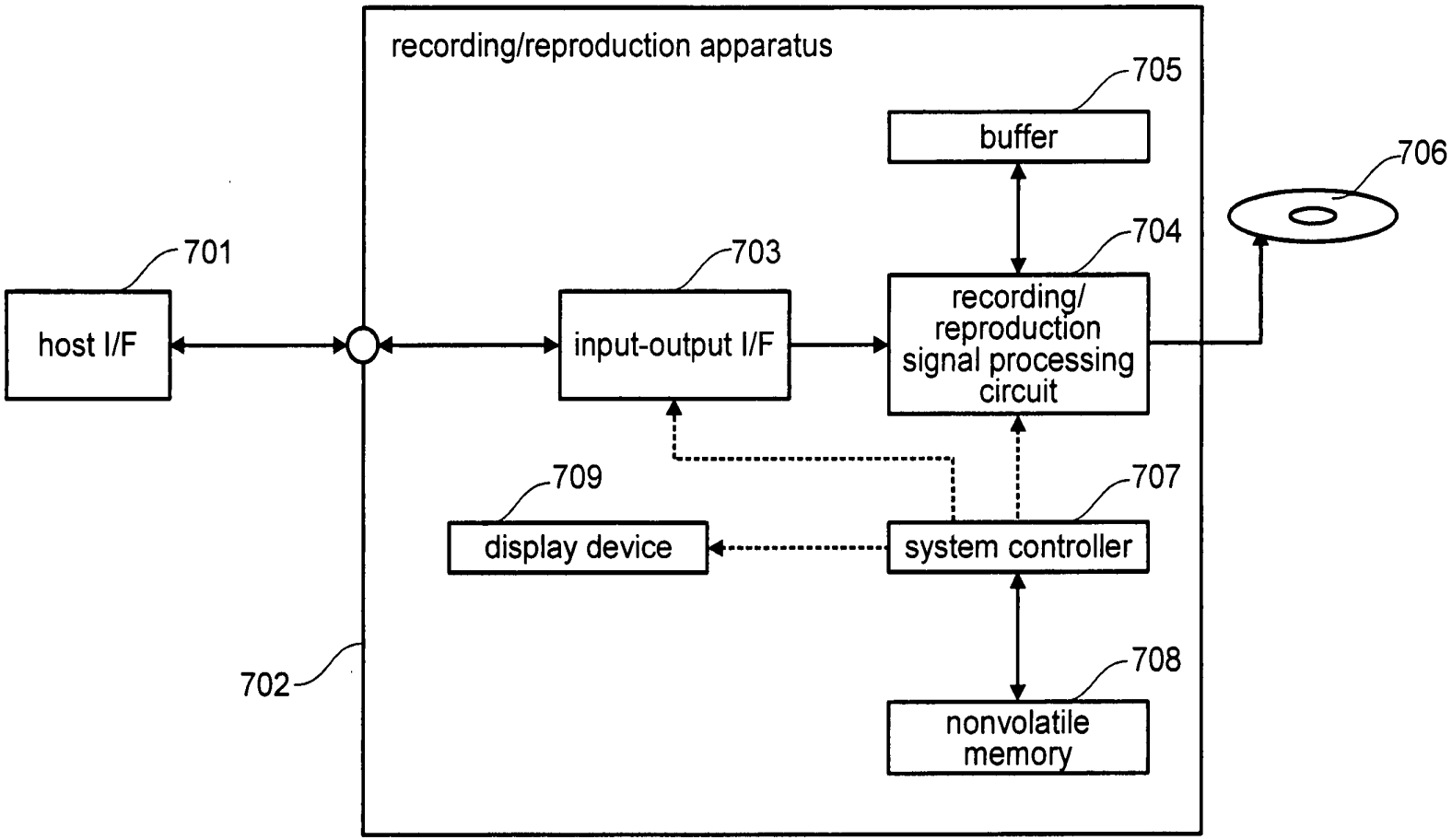
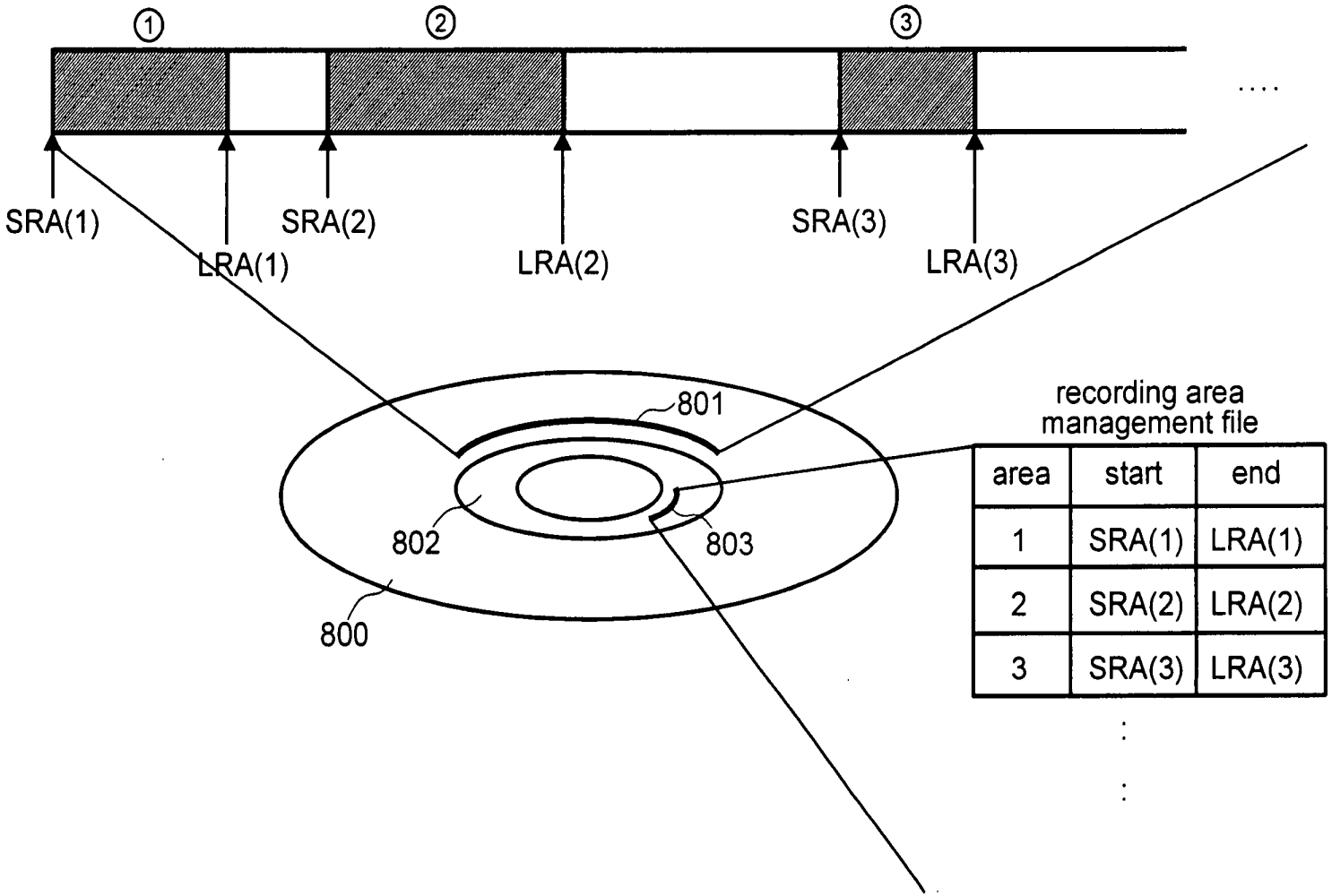

recording/reproduction apparatus
705
buffer
706
701
703
704
host I/F
input-output I/F
recording/
reproduction
signal processing
circuit
709
707
display device
system controller
702
708
nonvolatile
memory

FIG.8



area	start	end
1	SRA(1)	LRA(1)
2	SRA(2)	LRA(2)
3	SRA(3)	LRA(3)

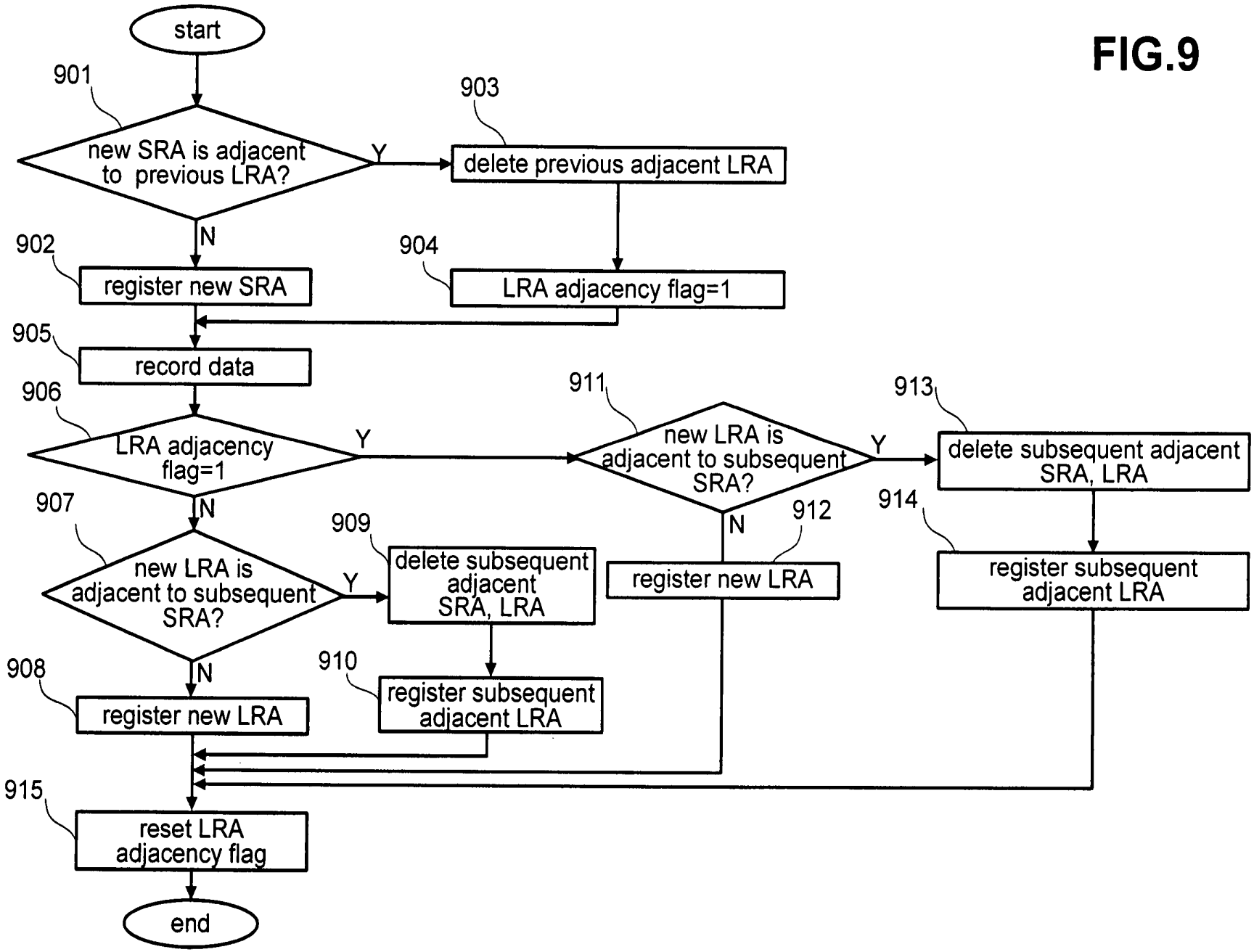

start
901
new SRA is adjacent to previous LRA?
Y
903
delete previous adjacent LRA
N
902
register new SRA
904
LRA adjacency flag=1
905
record data
906
LRA adjacency flag=1
Y
911
new LRA is adjacent to subsequent SRA?
Y
913
delete subsequent adjacent SRA, LRA
N
912
register new LRA
914
register subsequent adjacent LRA
907
new LRA is adjacent to subsequent SRA?
N
909
delete subsequent adjacent SRA, LRA
Y
908
register new LRA
N
910
register subsequent adjacent LRA
915
reset LRA adjacency flag
end

FIG.9

FIG.10

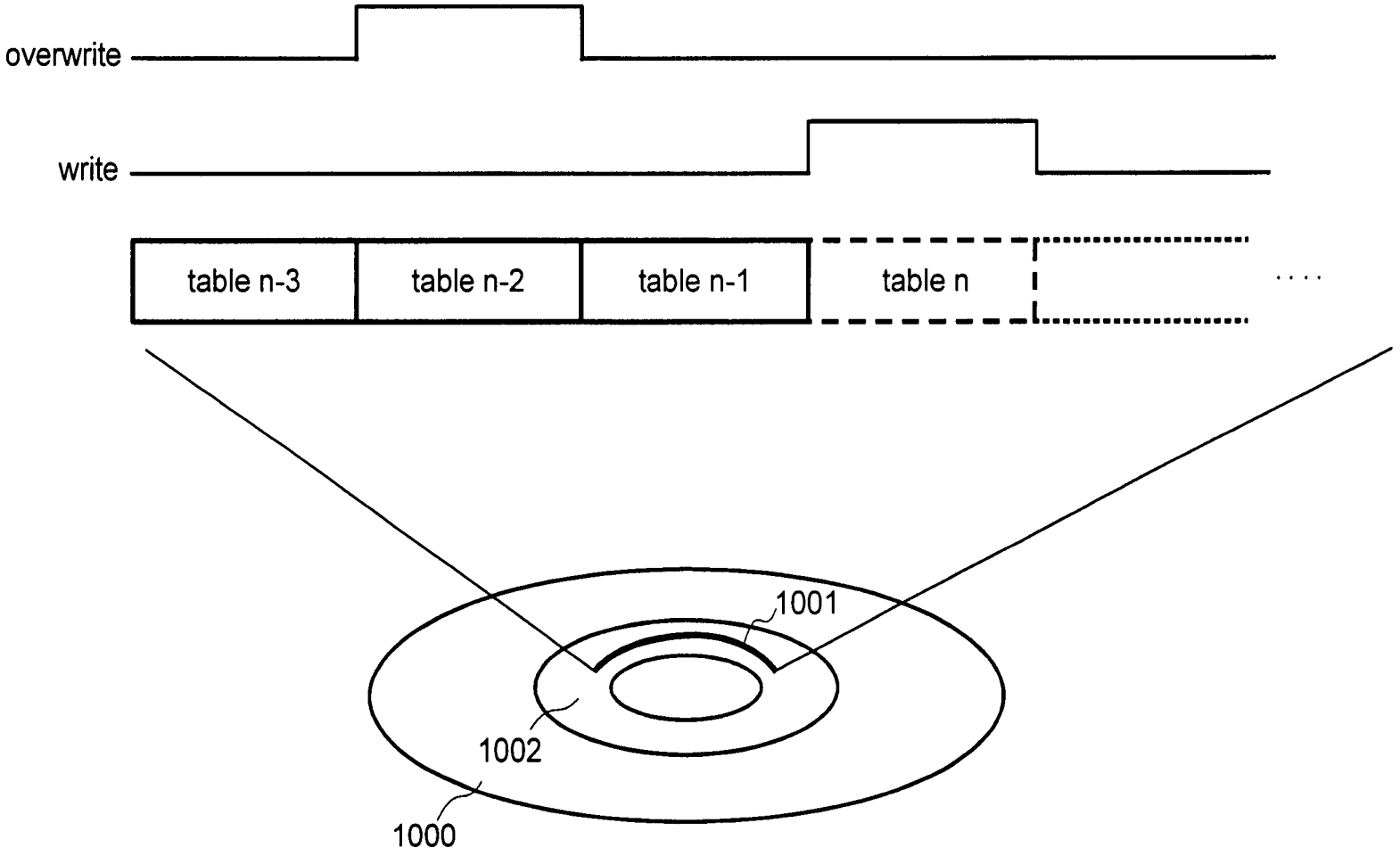

overwrite
write
table n-3
table n-2
table n-1
table n
1001
1002
1000

FIG.11

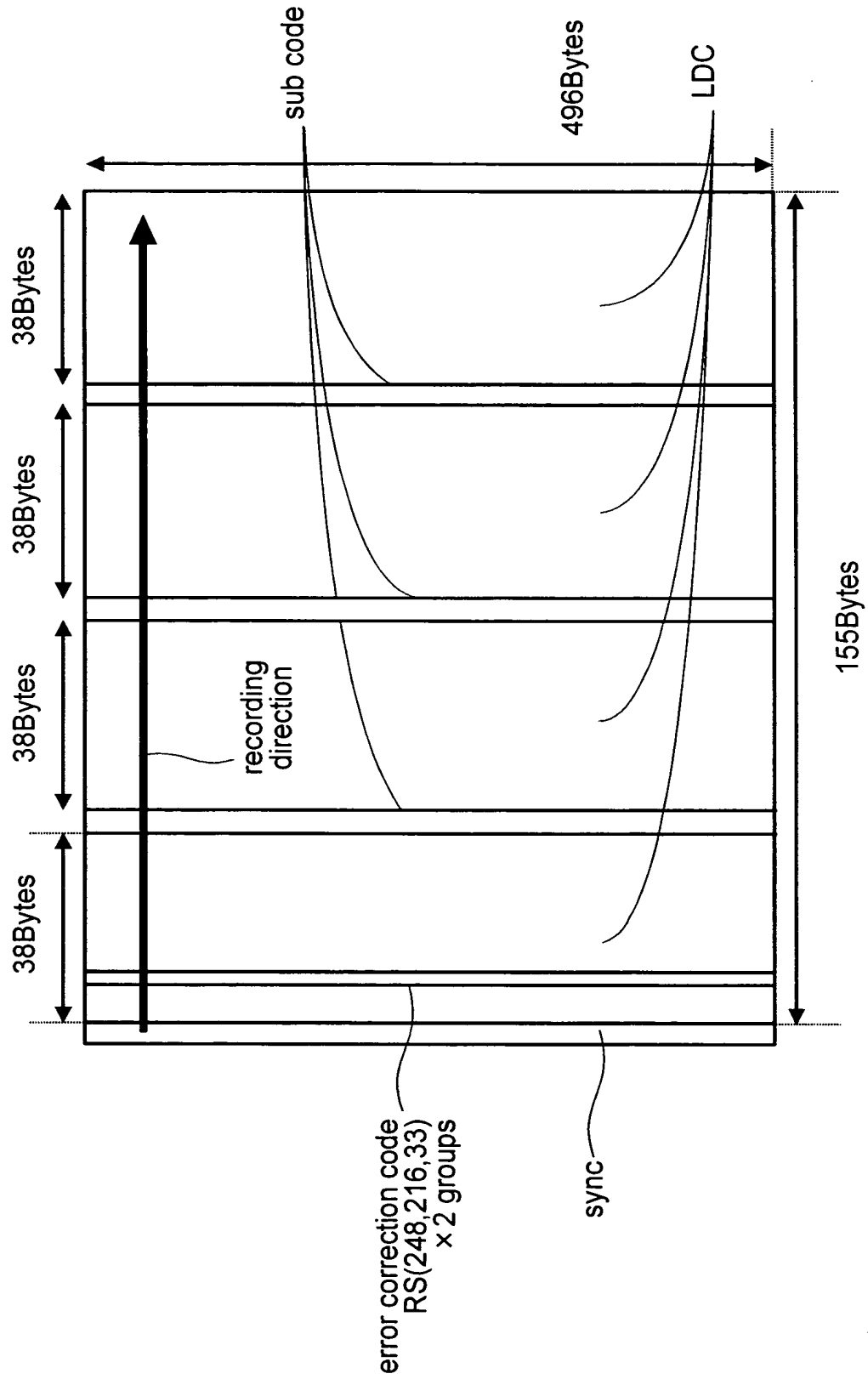

sub code
496Bytes
LDC
38Bytes
38Bytes
38Bytes
38Bytes
recording direction
155Bytes
error correction code RS(248,216,33) ×2 groups
sync

FIG.12

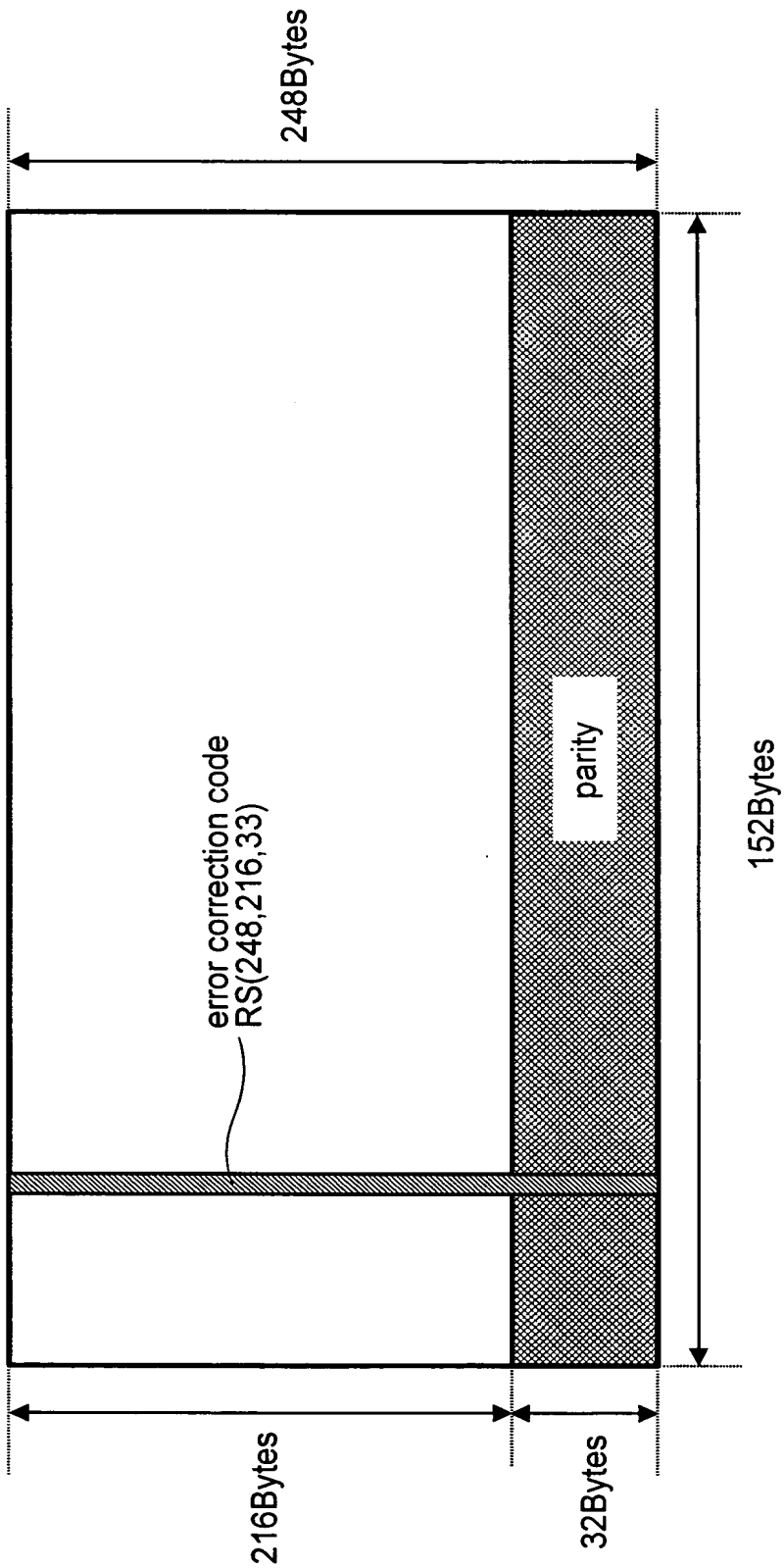
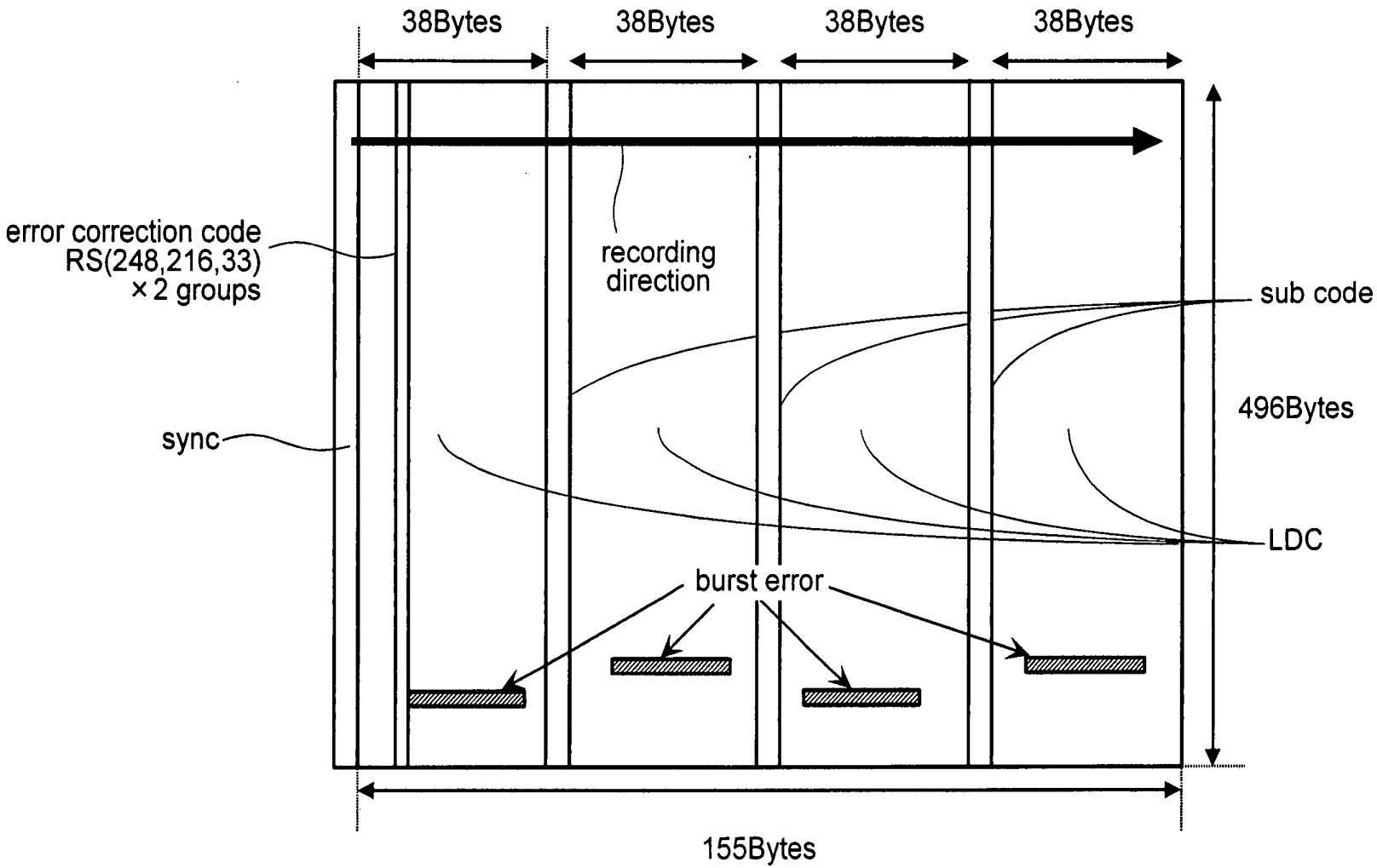

248Bytes
error correction code
RS(248,216,33)
parity
152Bytes
216Bytes
32Bytes

FIG.13


38Bytes
38Bytes
38Bytes
38Bytes
error correction code
RS(248,216,33)
× 2 groups
recording
direction
sub code
496Bytes
sync
LDC
burst error
155Bytes

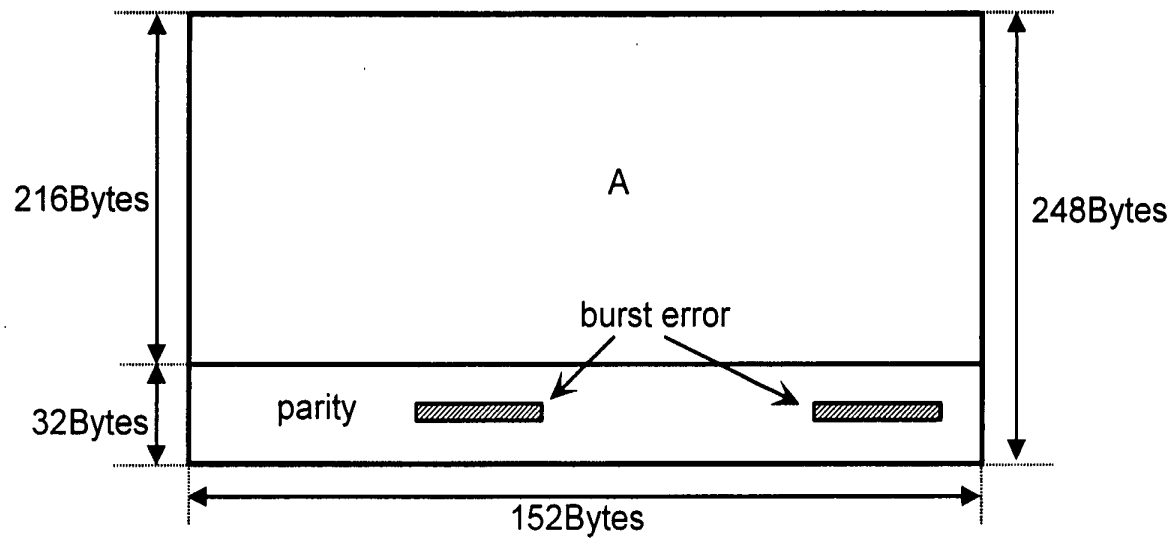

A
216Bytes
248Bytes
burst error
parity
32Bytes
152Bytes

FIG.14

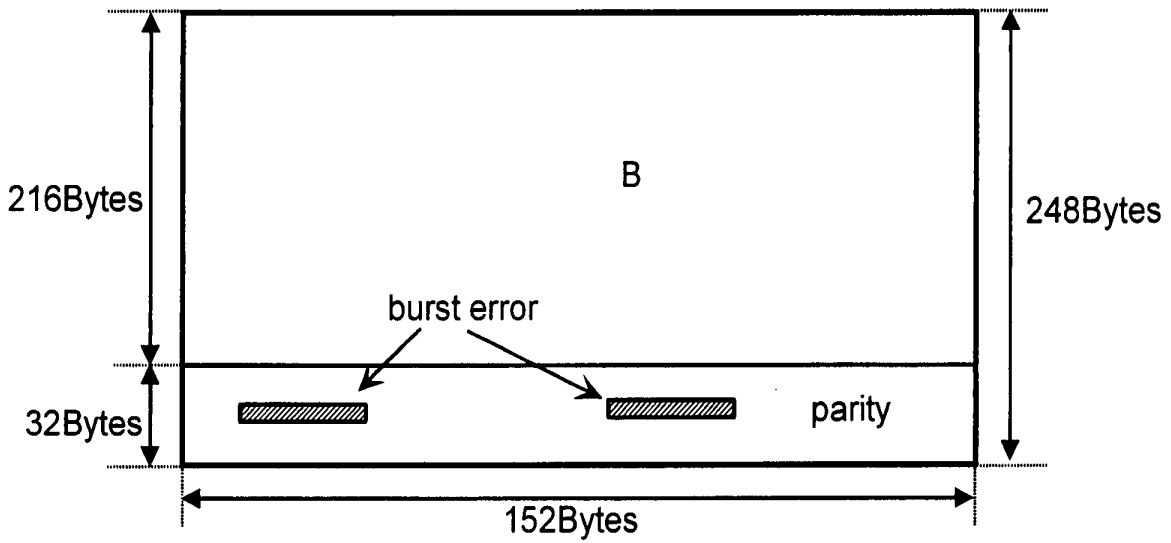
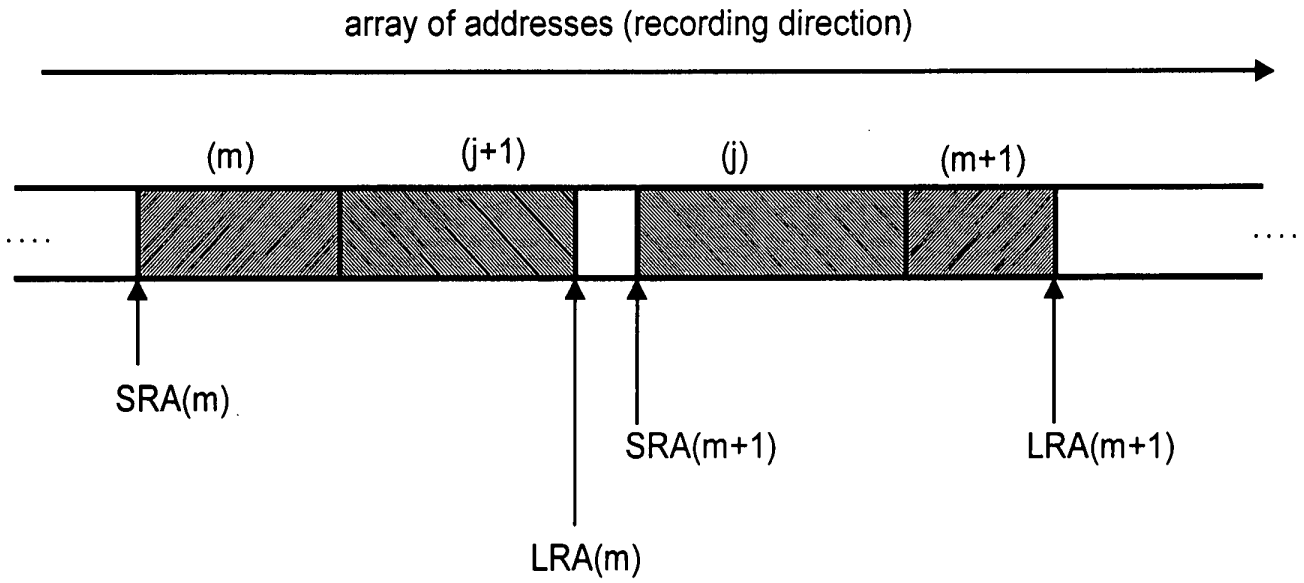

B
216Bytes
248Bytes
burst error
32Bytes
parity
152Bytes

FIG.15



area	start address	end address
m+(j+1)	SRA(m)	LRA(m)
j+(m+1)	SRA(m+1)	LRA(m+1)

FIG.16

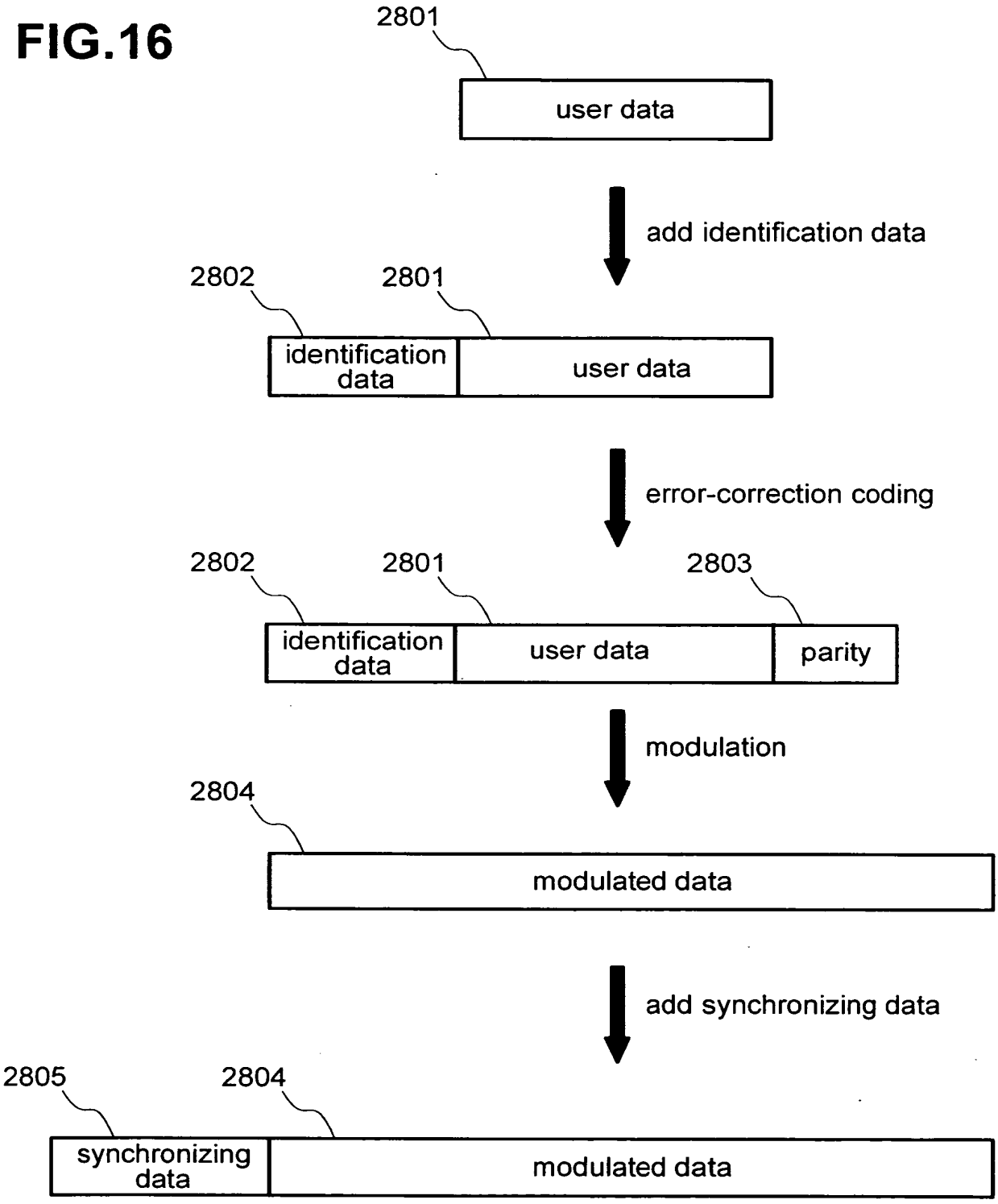

2801
user data
add identification data
2802
2801
identification data
user data
error-correction coding
2802
2801
2803
identification data
user data
parity
modulation
2804
modulated data
add synchronizing data
2805
2804
synchronizing data
modulated data

FIG.17

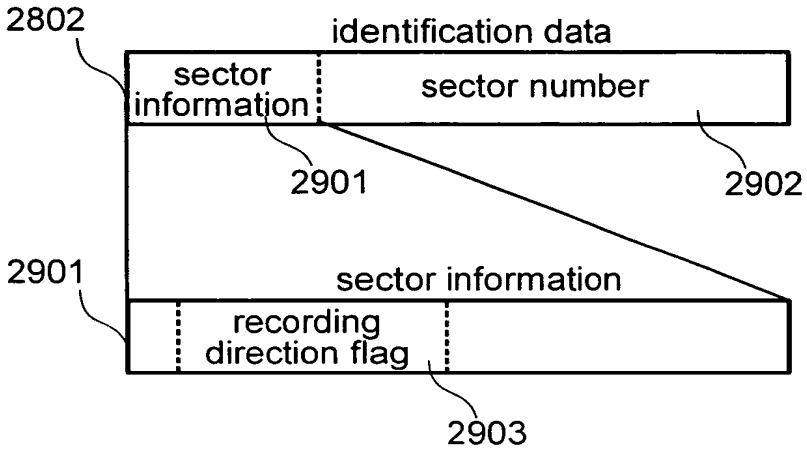

2802
identification data
sector information
sector number
2901
2902
2901
sector information
recording direction flag
2903

FIG.18

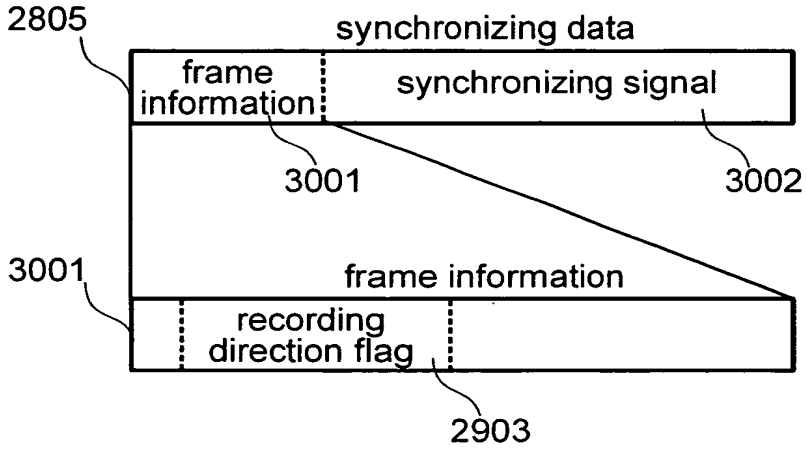

2805
synchronizing data
frame information
synchronizing signal
3001
3002
3001
frame information
recording direction flag
2903

FIG.19

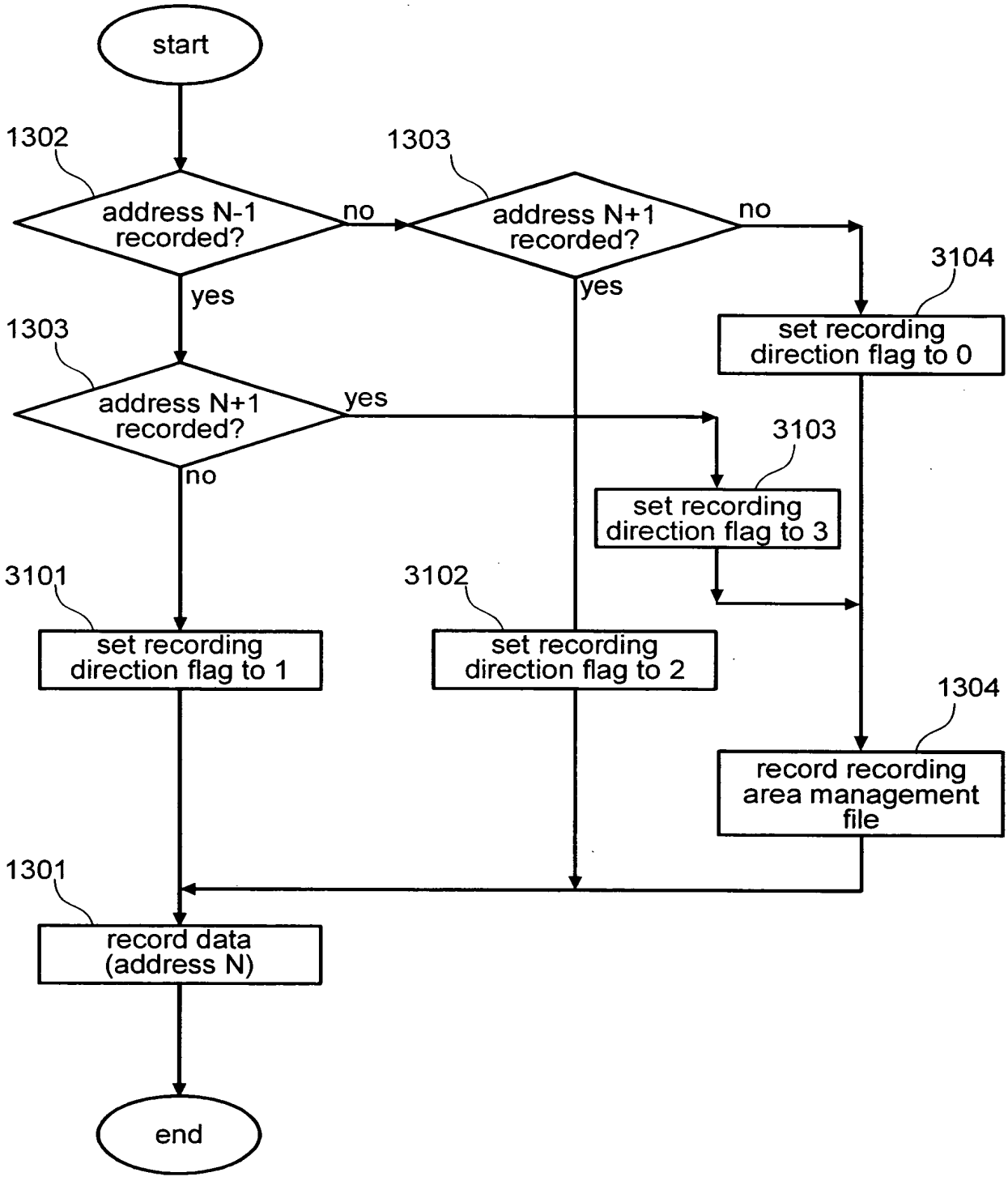

start
1302
address N-1 recorded?
no
1303
address N+1 recorded?
no
3104
set recording direction flag to 0
yes
yes
1303
address N+1 recorded?
yes
3103
set recording direction flag to 3
no
3101
set recording direction flag to 1
3102
set recording direction flag to 2
1304
record recording area management file
1301
record data (address N)
end

FIG.20

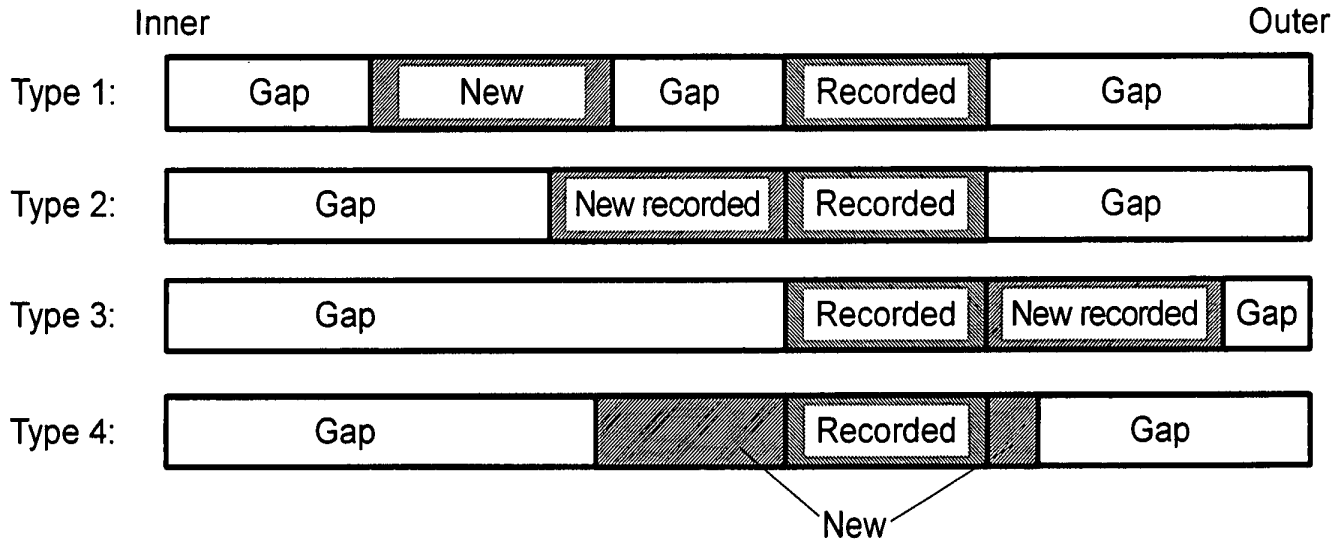

Inner
Outer
Type 1:
Gap
New
Gap
Recorded
Gap
Type 2:
Gap
New recorded
Recorded
Gap
Type 3:
Gap
Recorded
New recorded
Gap
Type 4:
Gap
Recorded
Gap
New

FIG.21

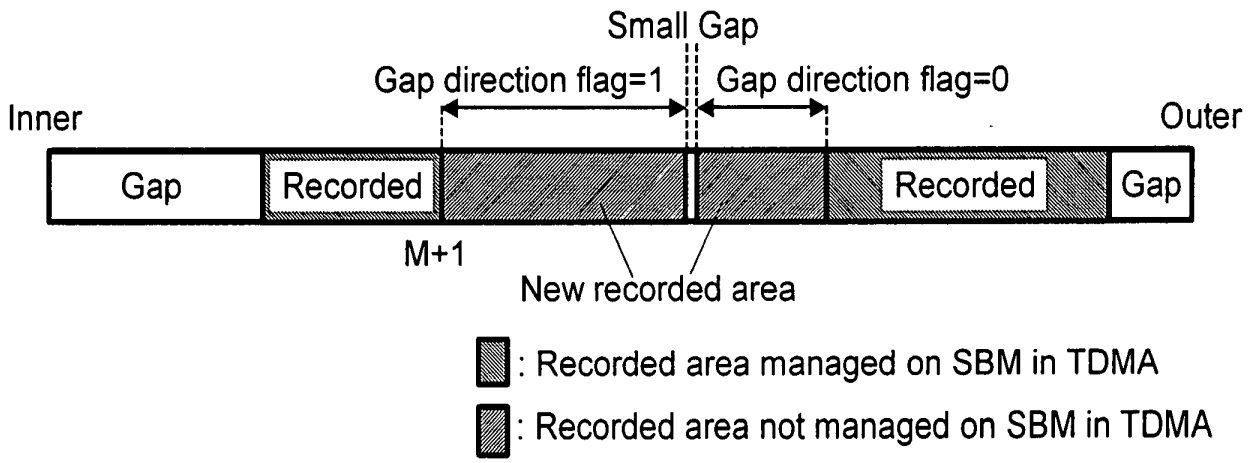

Small Gap
Gap direction flag=1
Gap direction flag=0
Inner
Outer
Gap
Recorded
Recorded
Gap
M+1
New recorded area
: Recorded area managed on SBM in TDMA
: Recorded area not managed on SBM in TDMA

FIG.22

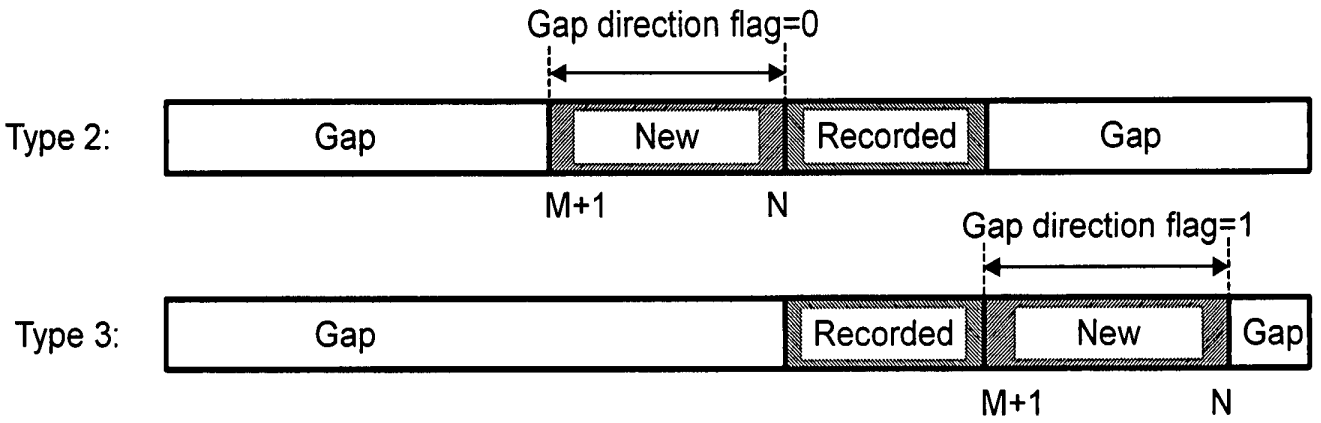
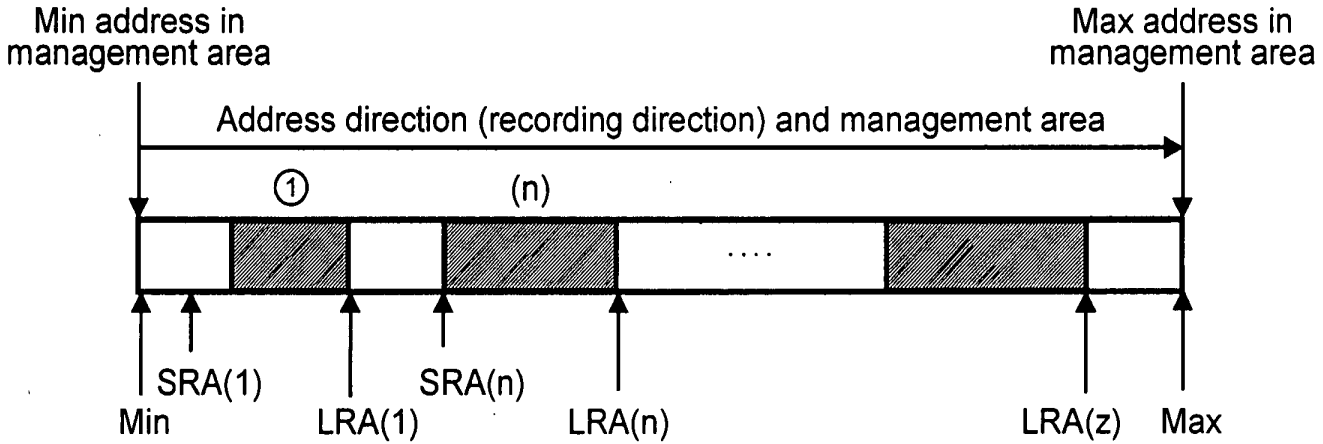

Gap direction flag=0
Type 2:
Gap
New
Recorded
Gap
M+1
N
Gap direction flag=1
Type 3:
Gap
Recorded
New
Gap
M+1
N

FIG.23



	start address	end address
start		start (Min)
1	SRA(1)	LRA(1)
2	SRA(2)	LRA(2)
3	SRA(3)	LRA(3)
:		
n	SRA(n)	LRA(n)
:		
:	:	LRA(z)
end	end(Max+1)	